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L10: Entry 5 of 11 File: USPT Aug 25, 1998

DOCUMENT-IDENTIFIER: US 5799196 A
TITLE: Method and apparatus of providing power management using a self-powered universal serial bus (USB) device

Brief Summary Text (11):
A USB host in the subject invention is coupled to a remote USB device located external to the computer. A first power source is coupled to a main power supply unit to provide power for the computer while the remote device receives power from a remote power supply unit coupled to a second power source. The host contains two types of logic: logic which can be powered down and logic which must be continually powered. Both types of logic are coupled to the main power supply unit so that they draw power from the first power source when the computer is operating normally. The continually-powered logic is also coupled to a control switch on the main power supply unit and further coupled to the remote power supply unit. When the computer enters suspend mode, the main power supply unit is turned off but the continually-powered logic remains active by drawing power from the second power source. When an external event occurs that requires processing by the computer, the remote USB device signals the continually-powered logic which then switches on the main power supply unit to resume the powered down logic.

Detailed Description Text (19):
In FIG. 1A, USB-compliant peripherals that generate external event signals, such as a keyboard, a mouse or a modem, are attached downstream to the remote hub 104A which provides full, operating power to those USB peripheral(s) that are bus-powered through remote power supply unit 108. One way to connect the remote power supply unit 108 to the second power source is to embed the remote hub 104A in a USB peripheral which has a direct and continuous AC connection. In one embodiment, the remote hub 104A is placed near the USB peripheral(s) that generate external event signals (mouse, keyboard, modem, etc.) to minimize cable lengths between the peripherals and their attachment points on the hub 104A. Since these types of USB peripherals are usually located near the computer cabinet, in this embodiment the remote hub 104A is embedded in a self-powered peripheral that is also near the computer, such as a set of external speakers. Other self-powered peripherals, such as a modem, are also good candidates to contain the remote hub 104A as will be apparent to those skilled in the art.

Detailed Description Text (21):
The continually-powered logic 110 in the USB host 100 is coupled to the main power supply unit 118 through two separate connections. One connection supplies power to the circuitry executing the continually-powered logic 110 during normal operations. The continually-powered logic 110 draws stand-by power through its attachment to the remote device 104A, 104B when the powered down logic 112 is in suspend mode and the main power supply unit 118 is turned off. The second connection between the continually-powered logic 110 and the main power supply unit 118 enables the continually-powered logic 110 to turn on the main power supply unit 118 to return full power to the host 100 upon receiving a resume signal from the remote device 104A, 104B or the occurrence of an event in the continually-powered logic 110, such as expiration of a timer. Power logic 114 is coupled to both the main power supply unit 118 and the remote power supply unit 108, and determines from which power supply unit the continually-power logic 110 draws its power. In this embodiment,

the power logic 114 is implemented in firmware, but can be implemented as hardware, part of the USB system software, or in a combination of components in the computer as will be apparent to those skilled in the art.

Detailed Description Text (24):
When the USB peripheral is suspended, it initiates remote wakeup resume signaling at block 214 and then waits (block 216) until it receives notice that the USB is fully awake before sending the data upstream (block 218). When the USB peripheral is remote function 104B, the resume signal is sent directly to the continually-powered logic 110. When the USB peripheral is attached to the remote hub 104A, the resume signal wakes-up the remote hub 104A. The remote hub 104A passes the resume signal upstream to the continually-powered logic 110, and downstream to any additional attached USB devices (block 214).

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L10: Entry 4 of 11 File: USPT Oct 19, 1999

DOCUMENT-IDENTIFIER: US 5968178 A
TITLE: Circuit and method for resetting a microcontroller

Detailed Description Text (4):
Referring to FIG. 2, a block diagram of a circuit 50 is shown in accordance with a preferred embodiment of the present invention. The circuit 50 generally comprises a low voltage detector block (or circuit) 52, an input power supply pin 54, a microcontroller 56 and an external input pin 58. The input power supply pin 54 may receive an input power supply voltage (e.g., VCC) that may be presented to an input 60 of the low voltage detector circuit 52 as well as to an input 62 of the microcontroller 56. The low voltage detector circuit 52 comprises an output 64 that may present a signal (e.g., an indication signal) to an input 66 of the microcontroller 56. The low voltage detector circuit 52 generally detects when the voltage present at the input power supply reaches a predetermined voltage level and then may present the indication signal to the microcontroller 56. The external input pin 58 may present a signal (e.g., a second indication signal) to an input 68 of the microcontroller 56. After the first indication signal is received at the input 66, the microcontroller 56 may enter into a suspend mode and then generally waits for the second indication signal to be received from the external input 58 which may indicate the microcontroller 56 should enter a run mode.

Detailed Description Text (8):
In addition to the cost, space and power savings of the circuit 50, an expanded implementation may result. For example, not all systems can tolerate the timer delay approach discussed in connection with FIG. 1. For example, in a Universal Serial Bus (USB) system (such as devices compliant with the USB Specification Version 1.0 published Jan. 15, 1996, the relevant sections of which are hereby incorporated by reference), devices may be "hot-plugged" into an already powered port on a host computer. In such a case, the power to the device may ramp and be stable at the device within a few microseconds, with signaling occurring within a few milliseconds. However, if the device is already plugged into the computer when power is applied to the computer, it may take as many as 100 ms to 1000 ms for the power supply to ramp to its final operating voltage. In this case, a single time-out time that can work for both extremes (i.e., long enough for proper functioning, yet short enough to allow signaling within the device specification) may not be practical or possible.

Detailed Description Text (9):
Devices may not require running immediately after power-up such as in the USB system for personal computers. After attachment of a USB peripheral device to a USB host computer, or with the power-up of an already attached device, the USB device generally waits for signaling from the host prior to the beginning of normal operation. In general, the USB communication begins with the second indication signal from the host to the USB device. The second indication signal may be presented in response to a Single Ended Zero (SEO) that persists for longer than 8 .mu.s. The USB device may only need to be in a known state (e.g., the suspend mode) after a Power On Reset (POR), and be ready to receive the second indication signal to begin operation. In this case, a USB device (such as the circuit 50 of FIG. 3) that powers up into the suspend mode may accomplish this readiness for both fast or slow ramping voltage supplies. The second indication signal may place the

L10: Entry 2 of 11 File: USPT Oct 17, 2000

DOCUMENT-IDENTIFIER: US 6134167 A
TITLE: Reducing power consumption in computer memory

Abstract Text (1):
A computer system comprising an input/output device, a processor, a memory device, and a bridge logic device for interfacing the memory device to the processor and input/output device incorporates a refresh logic device for generating a memory refresh signal during suspend mode. Because the rate at which memory must be refreshed generally depends on the temperature of the memory device, the refresh logic varies the frequency of the refresh signal according to the temperature of the memory device, resulting in substantial power savings. In a preferred embodiment, the refresh logic uses a normal-rate refresh signal at the beginning of suspend mode and incrementally steps down the refresh rate as the memory temperature decreases. In other embodiments, the refresh logic incorporates a signal generator which produces a refresh signal at a frequency that varies according the output voltage from a temperature sensor or the temperature-sensitive resistance of a thermistor. In yet another embodiment, a variable-rate refresh logic is incorporated into the memory device, resulting in a self-refreshing memory module.

Detailed Description Text (48):
Because the CPU 102 is idle during suspend mode, however, it is incapable of determining when one hour has elapsed. Therefore, I/O controller 130 monitors the state of the Real-Time Clock 131, after suspend mode commences. When the value of the RTC 131 indicates that the predetermined wait time (preferably one hour) has passed, the I/O controller 130 wakes up computer system 100 by deasserting the suspend signal. Immediately after the computer system 100 begins operating, I/O controller 130 transmits an SMI signal to the CPU 102 to direct the CPU 102 to reduce the refresh rate. In response to the SMI, the CPU 102 asserts the select signal, which slows the frequency of the refresh signal by a factor of n. After the refresh logic 550 begins refreshing memory at the slower rate, the I/O controller 130 then reasserts the suspend signal to again shut down the computer system 100. Afterward, the main memory 106 receives a refresh signal whose frequency is reduced by a factor of n, resulting in power savings proportional to n.

CLAIMS:

23. In a computer system having a processor receiving input signals from an input device and a memory device that stores data, a method of reducing power consumption in the computer system comprising:

operating the computer system in a low power mode of operation, and while the computer system is in a low power mode of operation;

providing a periodic refresh signal to the memory device; and

slowing the rate of the periodic refresh signal to slow the refresh rates of the memory device as the memory device becomes able to retain data with a slower refresh rate.

L2: Entry 1 of 7 File: USPT Jul 20, 1999

DOCUMENT-IDENTIFIER: US 5926828 A
** See image for Certificate of Correction **
TITLE: Method and apparatus for controlling data transfer between a synchronous DRAM-type memory and a system bus

CLAIMS:

1. A method of controlling data flow between a memory and a device comprising the steps of:

receiving a data transfer request in the form of a read request to read data from the memory or in the form of a write request to write data into the memory;

asserting a read/write command in response to the data transfer request to set a burst start address indicating where the data will be transferred to in the memory in response to the write request or indicating where the data will be transferred from in response to the read request;

(1) in response the read request:

(a) transferring a first portion of the data from the burst start address to the device;

(b) initiating transfer of a second portion of the data from addresses immediately subsequent to the burst start address to the device;

(c) in response to the device not being ready to receive the second portion of the data from the memory, asserting a hold signal to a memory controller to suspend the data transfer, the memory controller latching a last address from which the second portion of the data was to be transferred from the memory; and

(d) in response to the data being ready to be transferred from the memory, deasserting the hold signal to the memory controller and resuming data transfer from the last address; and

(2) in response to the write request:

(a) transferring a third portion of the data to the burst start address from the device;

(b) initiating transfer of a fourth portion of the data from the device to addresses immediately subsequent to the burst start address;

(c) in response to the fourth portion of the data not being ready, asserting a hold signal to the memory controller to suspend data transfer indicating that the device is not ready to send data, the memory controller latching a further last address to which the fourth portion of the data was to be transferred to in the memory, sending a masking signal from a mask generator in response to the hold signal to the memory to avoid data transfer to the further last address; and,

(d) in response to data being ready, deasserting the hold signal to the memory controller and resuming data transfer to the further last address to which the fourth portion of the data was to be transferred.

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L2: Entry 2 of 7 File: USPT Sep 29, 1998

DOCUMENT-IDENTIFIER: US 5815285 A
TITLE: Facsimile device with user-friendly automatic receive mode

Detailed Description Text (2):
Reference should now be made to FIG. 1, which is a block diagram showing how a facsimile 10 and other receiving devices such as a telephone 12 and telephone answering machine 14 may be connected in conventional fashion to a communications line 16. In particular, note that the telephone 12 is connected in parallel with the facsimile 10, thereby permitting either device to go "off-hook" and send a signal to the telephone company's central office (not shown) that the device is ready to answer the incoming call and that the ringing should stop. Accordingly, in such a parallel arrangement, either device may answer a call whether any other device is connected and operational. In contrast, the telephone answering machine 14 is connected to the communications line 16 by means of a series connection via the facsimile 10 (that is, it is "downstream" from the facsimile 10), and accordingly, the facsimile 10 can control the functioning of the telephone answering machine 14, for example by temporarily disconnecting the telephone answering machine 14 from the line if the facsimile 10 detects a CNG tone on the communications line 16 representative of an incoming facsimile transmission.

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L2: Entry 6 of 7 File: DWPI Jul 28, 2004

DERWENT-ACC-NO: 2003-393848
DERWENT-WEEK: 200449

TITLE: Selective suspension of bus devices e.g. for computers, which employs signal and wait technique to assert power control over hardware devices

Basic Abstract Text (1):
NOVELTY - Method includes signaling and waiting to suspend a peripheral device connected to a computer. The peripheral device sends an idle request to the computer when the peripheral device is ready to suspend. The peripheral device then waits to receive a call from the computer to a call back function associated with the peripheral device to suspend the peripheral device.

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L5: Entry 1 of 3 File: USPT May 11, 2004

DOCUMENT-IDENTIFIER: US 6735713 B1
TITLE: System for suspending current bus cycle of microprocessor upon receiving external bus retry signal for executing other process and re-staring the suspended bus cycle thereafter

Brief Summary Text (13):
The system including a microprocessor of the present invention comprises a bus retry output device for outputting a bus retry signal and a microprocessor including a bus retry detection part for determining whether or not a bus retry signal is input from the bus retry output device and a bus cycle controller for suspending a currently executed bus cycle in response to the bus retry signal detected by the bus retry detection part and for re-starting the suspended bus cycle.

Detailed Description Text (10):
In this manner, in the MPU 10 of the present invention, even when an interrupt request with higher priority is issued from the audio chip 86 while a READY signal is being waited to be returned from the video chip 84, the interrupt process of the audio chip 86 can be executed by suspending the bus cycle for the video ship 84. Accordingly, the audio processing cannot be delayed due to the influence of the processing time of the video chip 84, so that the conventional problems of skipped notes and sound out of rhythm can be prevented. In addition, such processes can be conducted by using hardware alone, and hence they can be executed rapidly and definitely.

Detailed Description Text (14):
Furthermore, the device for outputting a BRTY signal is not limited to the bridge chip but can be any device external to the microprocessor. However, since it is necessary to compare a currently executed bus cycle and an interrupt request so as to determine whether or not the currently executed bus cycle should be or can be suspended, a device capable of supervising the bus of the microprocessor is used.

L10: Entry 1 of 11 File: USPT Jan 20, 2004

DOCUMENT-IDENTIFIER: US 6681334 B2
TITLE: Disk sensor power system for sampling output signal of disk sensor at predetermined moments related to power saving state

Detailed Description Text (17):
This high output from the disk sensor means 12 correctly indicates that there is a disk cartridge loaded on the turntable 11 at the moment of t.sub.6, but not whether this cartridge is the same as the one that was loaded before t.sub.5 or is a different one that was reloaded in the course of the t.sub.2 -t.sub.6 SUSPEND state, as at t.sub.4, of the SUSPEND/RESUME signal, that is, not whether a disk change has been made during that SUSPEND period. The interface 5 according to the present invention is well equipped to distinguish between these two possible cases, accurately discerning the occurrence, as in this case, or nonoccurrence of a disk change during each SUSPEND period. Additionally, the interface 5 according to the invention is enabled to ascertain any of such possible histories of disk loading and unloading immediately when the SUSPEND/RESUME signal regains a RESUME state, as at t.sub.5 in FIG. 2, without waiting for the appearance of stepping pulses.

CLAIMS:

5. A rotating disk data storage system operating under the control of a processor, comprising: (A) a data storage device comprising: (a) a transducer for data transfer with a rotating data storage disk being held in a preassigned position; and (b) disk sensor means for providing an output signal indicative of whether a data storage disk is in the preassigned position or not; and (B) an interface for connecting the data storage device to a processor, the interface comprising: (a) power-saving means for generating a power-saving signal under the direction of the processor, the power-saving signal having a power-saving state, indicative of the fact that the data storage device is in a power-saving state, and a non-power-saving state indicative of the fact that the data storage device is not in a power-saving state; (b) drive select means for generating a drive select signal under the direction of the processor, the drive select signal having a select state, indicative of the fact that the data storage device is chosen for data transfer with the rotating data storage disk, and a not-select state indicative of the fact that the data storage device is not, the select state of the drive select signal beginning after the beginning of each non-power-saving state of the power-saving signal; (c) sampling means connected to the disk sensor means and the power-saving means and the drive select means for sampling the output signal of the disk sensor means at a plurality of different moments that are predetermined in relation to each power-saving state of the power-saving signal, the predetermined moments including a first moment approximately at the beginning of each power-saving state of the power-saving signal, a second moment approximately at the end of each power-saving state of the power-saving signal, and a third moment approximately at the beginning of each select state of the drive select signal; and (d) disk status means connected to the sampling means for ascertaining a history of disk loading and unloading past each power-saving state of the power-saving signal on the basis of the three samples of the output signal of the disk sensor means.

9. A rotating disk data storage system operating under the control of a processor, comprising: (A) a data storage device comprising: (a) a transducer for data

transfer with a rotating data storage disk being held in a preassigned position; and (b) disk sensor means for providing an output signal indicative of whether a data storage disk is in the preassigned position or not; and (B) an interface for connecting the data storage device to a processor, the interface comprising: (a) power-saving means for generating a power-saving signal under the direction of the processor, the power-saving signal having a power-saving state, indicative of the fact that the data storage device is in a power-saving state, and a non-power-saving state indicative of the fact that the data storage device is not in a power-saving state; (b) the output signal of the disk sensor means of the data storage device being correctly representative of disk presence or absence both when the power-saving signal is in the non-power-saving state and as long as no disk change is made during the power-saving state of the power-saving signal, and, in the event of a change from one disk to another during the power-saving state of the power-saving signal, being indicative of disk absence from the moment said one disk was unloaded to, at the earliest, the moment the power-saving signal subsequently gains a non-power-saving state; (c) drive select means for generating a drive select signal under the direction of the processor, the drive select signal having a select state, indicative of the fact that the data storage device is chosen for data transfer with the rotating data storage disk, and a not-select state indicative of the fact that the data storage device is not the select state of the drive select signal beginning after the beginning of each non-power-saving state of the power-saving signal; (d) first sample memory means connected to the disk sensor means for storing a sample of the output signal thereof at the end of each non-power-saving state of the power-saving signal at the latest; (e) second sample memory means connected to the disk sensor means for storing a sample of the output signal thereof at the end of each power-saving state of the power-saving signal at the earliest; (f) third sample memory means connected to the disk sensor means for storing a sample of the output signal thereof at the beginning of the select state of the drive select signal; and (g) disk status means connected to the first, the second and the third sample memory means for ascertaining a history of disk loading and unloading past each power-saving state of the power-saving signal on the basis of the three samples of the output signal of the disk sensor means stored on the sample memory means.

12. A rotating disk data storage system operating under the control of a processor, comprising: (A) a data storage device comprising: (a) a transducer for data transfer with a rotating data storage disk being held in a preassigned position; and (b) disk sensor means for providing an output signal indicative of whether a data storage disk is in the preassigned position or not; and (B) an interface for connecting the data storage device to a processor, the interface comprising: (a) power-saving means for generating a power-saving signal under the direction of the processor, the power-saving signal having a power-saving state, indicative of the fact that the data storage device is in a power-saving state, and a non-power-saving state indicative of the fact that the data storage device is not in a power-saving state; (b) the output signal of the disk sensor means of the data storage device being correctly representative of disk presence or absence both when the power-saving signal is in the non-power-saving state and as long as no disk change is made during the power-saving state of the power-saving signal, and, in the event of a change from one disk to another during the power-saving state of the power-saving signal, being indicative of disk absence from the moment said one disk was unloaded to, at the earliest, the moment the power-saving signal subsequently gains a non-power-saving state; (c) drive select means for generating a drive select signal under the direction of the processor, the drive select signal having a select state, indicative of the fact that the data storage device is chosen for data transfer with the rotating data storage disk, and a not-select state indicative of the fact that the data storage device is not, the select state of the drive select signal beginning after the beginning of each non-power-saving state of the power-saving signal; (d) first sample memory means connected to the disk sensor means for storing a sample of the output signal thereof between the end of the select state of the drive select signal and the end of each non-power-saving state

of the power-saving signal; (e) second sample memory means connected to the disk sensor means for storing a sample of the output signal thereof between the end of each power-saving state of the power-saving signal and the end of each not-select state of the drive select signal; (f) third sample memory means connected to the disk sensor means for storing a sample of the output signal thereof at the beginning of the select state of the drive select signal; and (g) disk status means connected to the first, the second and the third sample memory means for ascertaining a history of disk loading and unloading past each power-saving state of the power-saving signal on the basis of the three samples of the output signal of the disk sensor means stored on the sample memory means.

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L11: Entry 4 of 4 File: DWPI Oct 30, 2001

DERWENT-ACC-NO: 2001-662358
DERWENT-WEEK: 200176

TITLE: Data communication method for software applications, involves transferring flag from USB device to USB host when USB device has not received data for specified time, and stopping data request when USB host receives flag

Basic Abstract Text (1):
NOVELTY - The data from the universal serial bus (USB) device (14) is transferred to the USB host (12) in response to data requests from the host. A flag is transferred from the USB device to the USB host when the USB device has not received the data for a predetermined time and data request is stopped when the USB host receives the flag.

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L11: Entry 3 of 4 File: USPT Aug 15, 2000

DOCUMENT-IDENTIFIER: US 6105097 A
TITLE: Device and method for interconnecting universal serial buses including power management

Detailed Description Text (18):
FIG. 5 is a state diagram illustrating a method 160 in accordance with another aspect of the invention for a peripheral device driver to coordinate/control the power manager of the USB-to-USB device. In particular, the drivers may desire to control the temporary halting of the clocks and/or the switching of the power. To accomplish this level of control, the power manager and the USB-to-USB device may request the permission to go into the suspended state from the opposite buses device driver as soon as the USB-to-USB device detects a suspend state on either of the USBs connected to the USB-to-USB device.

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L24: Entry 2 of 4 File: USPT Aug 25, 1998

DOCUMENT-IDENTIFIER: US 5799196 A
TITLE: Method and apparatus of providing power management using a self-powered universal serial bus (USB) device

Detailed Description Text (24):
When the USB peripheral is suspended, it initiates remote wakeup resume signaling at block 214 and then waits (block 216) until it receives notice that the USB is fully awake before sending the data upstream (block 218). When the USB peripheral is remote function 104B, the resume signal is sent directly to the continually-powered logic 110. When the USB peripheral is attached to the remote hub 104A, the resume signal wakes-up the remote hub 104A. The remote hub 104A passes the resume signal upstream to the continually-powered logic 110, and downstream to any additional attached USB devices (block 214).

L10: Entry 6 of 11 File: USPT Apr 7, 1998

DOCUMENT-IDENTIFIER: US 5736873 A
TITLE: Power saving control circuit for a display apparatus

Brief Summary Text (12):
The horizontal and vertical sync signals generated for managing the power of the computer's peripheral equipment corresponding to the use or non-use computer system as described above are referred to as power management signals.

Brief Summary Text (13):
Korean Patent Application No. 93-5332, corresponding to U.S. Pat. No. 5,483,464, filed by the same applicant of this patent application discloses a technique entitled "Power Saving Apparatus of Peripheral Equipments supplied to a Computer", in which power of the computer's peripheral equipment is economized by means of the power management signals suggested in the above-mentioned "DPMS Proposal" of the VESA.

Brief Summary Text (17):
In use or non-use the demand, the same applicant of this patent application filed Patent Application No. 93-15279 corresponding to U.S. patent application Ser. No. 08/283,759 entitled: "Power Management Signal Generating Method and Control Apparatus of Peripheral Equipments of a Computer in a Computer system".

Detailed Description Text (32):
After the output signal e or h from the vertical or horizontal frequency discriminator 14 and 18 is supplied as the reset signal to the reset terminal of the counter 90 via the NAND gate 94, the counter 90 counts the clock signal from the clock demultiplier 10. If the reset signal is not supplied for the predetermined time set in the counter 90, the counter 90 supplies the output signal of high level to the decoder 24 while allowing the output signal to be of low level if the reset signal is supplied within the predetermined time of performing the counting operation. Accordingly, the vertical and horizontal no-signal checking units 22 and 28 which are delay means for making the outputs of the vertical and horizontal frequency discriminators 14 and 18 wait for seconds accurately determines the state of the monitor for approximately 5 seconds. The reason for waiting for approximately 5 seconds is to instantly display the picture when the mode is converted to the On state within 5 seconds or so after blanking the picture to eliminate the stand-by time, since the signal output of high level from the horizontal no-signal checking unit 28 resulting from the power saving mode (suspend state and off state) has the same effect of turning off a power switch (not shown) of the monitor, roughly tens of seconds are required for displaying the picture in spite of switching to the On state by receiving the horizontal or vertical sync signal again.

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L11: Entry 2 of 4 File: USPT Aug 7, 2001

DOCUMENT-IDENTIFIER: US 6272644 B1
TITLE: Method for entering powersave mode of USB hub

Detailed Description Text (11):
In a typical USB system having a USB hub (11) connected to a host computer and a plurality of peripheral devices a suspend request from the host computer is passed to the USB hub (11). The USB hub passes this request to the USB peripheral devices. The USB hub (11) also tells the microcontroller to suspend. The microcontroller responds to this suspend request by instructing the USB hub (11) to suspend itself by suspending its clock using a stop clock signal. The microcontroller then asynchronously turns its own clock off.

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L24: Entry 1 of 4 File: USPT Jul 4, 2000

DOCUMENT-IDENTIFIER: US 6085325 A
** See image for Certificate of Correction **
TITLE: Method and apparatus for supporting power conservation operation modes

Detailed Description Text (10):
control circuit 242 detects activity on the USB 240. The microcontroller 301 defines a window of time in which it waits for the activity signal from the suspend control circuit 242. If the microcontroller 301 does not receive an activity signal during the window of time, it sends a suspend signal to the suspend control circuit 242 indicating that the USB device 241 should be put into a suspend state. When operating in the suspend state, the USB device 241 reduces its power consumption by disabling the clock in suspend control circuit 242 and oscillator unit 302 in the USB device 241. Disabling the clock in suspend control circuit 242 and oscillator unit 302 puts the USB device 241 in a static state where current consumption comes only from current leakage from the components in the USB device 241.

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L22: Entry 2 of 4 File: USPT May 20, 2003

DOCUMENT-IDENTIFIER: US 6567921 B1
TITLE: Asynchronous low power mode bus controller circuit and method of low power mode operation

Brief Summary Text (10):
The present invention provides an asynchronous logic circuit that suspends the clock in a bus controller and places the device in low power mode. The asynchronous logic circuit functions as an event detector and responder not requiring clocks. While in low power mode, bus events can be detected and reported to the bus controller after wake up is complete. Additionally, the asynchronous logic circuit can respond to bus events until the bus controller is fully powered and ready to take over control.

Current US Cross Reference Classification (1):
713/601

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L22: Entry 3 of 4 File: USPT Oct 31, 2000

DOCUMENT-IDENTIFIER: US 6141711 A
TITLE: Method and apparatus to enable insertion/ejection of a device in a computer system while maintaining operation of the computer system and application software

Abstract Text (1):
A secondary bus controller allows for hot insertion and ejection of devices from the secondary bus without ceasing operations or halting software in the host computer. When a device is to be inserted a signal is sent to the secondary bus controller. The secondary bus controller suspends operation of the secondary bus, placing devices on the secondary bus in stasis. An interrupt handler reconfigures the system for the newly inserted card once it has been inserted. Attempts to access devices on the secondary bus during the insertion process may be met with a retry signal until insertion is complete. The ejection process follows similar steps, isolating and suspending operations on the secondary bus and triggering an interrupt routine in the host processor to reconfigure the system. The host processor and primary busses, along with the secondary bus controller remain active throughout the insertion or ejection processes. Thus, applications running on the host computer need not be terminated during insertion or ejection. The present invention has particular application to network server computer systems.

Current US Cross Reference Classification (1):
713/601

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